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IB75B-AHS TP75 REV 6.0

CPU:

Intel Sandy/Ivy Bridge processors in LGA1155 Package 95W

System Chipset: B75

Main Memory:

Dual Channel/DDR-III*2(Max 16GB) 1066/1333

Onboard Device:

Super I/O:IT8728F-EX

LAN:Realtek 8111F

HD Codec:ALC662 3 jacks

Power solution:

CPU Voltage Regulators:3phase by ISL6363

VTT voltage Regulators:1Phase by uP1514

DDR voltage Regulators:1Phase by uP1514

Expansion Slots:

PCI EXPRESS 16X SLOT*1

PCI EXPRESS 4X SLOT*1

PCI EXPRESS 1X SLOT*2

PCI SLOT*2

REAR IO:

PS/2 Port

COM Port

2 layer USB2.0 Port

2 layer USB3.0 Port

2 layer USB2.0 + Gb RJ-45 Ports

Audio Jacks

Front I/O:

SATA3 * 1

SATA2 * 5

USB Header * 2

CPU /System1

PRINT Header

Front Audio Header & SPDIF Out 1

I/O Panel:

TBD

HW Engineer		Date	
HW Leader1		Date	
HW Leader2		Date	

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V0.6 TO V6.0:

PAGE14. Change SATA CONN

PAGE17. Delete R,G,B resistor to GND

PAGE23. Change PEX16_2 to PCIEX16-164 PIN-R

PAGE31. Change LL1 to INDUCTOR 4.7UH 880mA SMD

PAGE38. Change +3V3_DUAL,+3V3_AUX VREF

PAGE39. Change SB_3V3REF, V_1P05_PCH,V_1P8_SFR VREF

PAGE41. Change V_VCCIO_VSA FB circuit

PAGE42. Change VCORE OCP,pull high PWM pin32 to +12V_AUX

PAGE43. Change curret balance

PAGE43. Change V_1P05_ME VREF,change C100 to Q39.B

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Title CHANGE LIST		
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DQ REMAPPING IMPLEMENTED
TO IMPROVE BREAKOUT AND
MINIMIZE CH-2-CH COUPLING

DQ REMAPPING IMPLEMENTED
TO IMPROVE BREAKOUT AND
MINIMIZE CH-2-CH COUPLING

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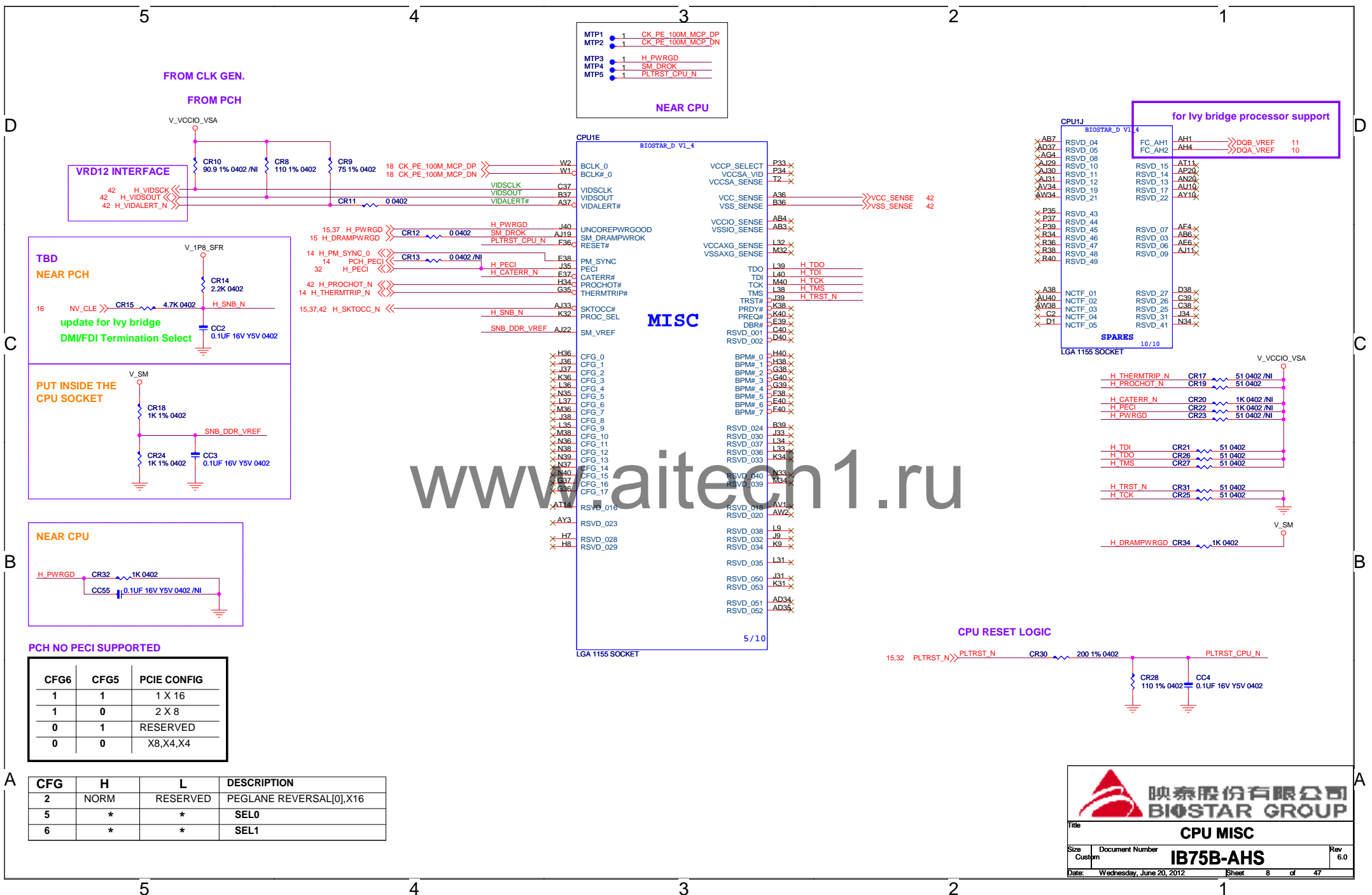
DDR_1
2/10

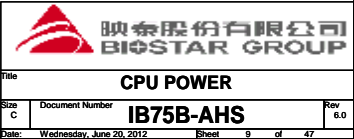
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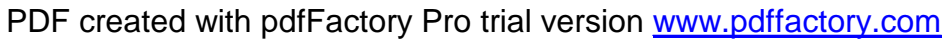
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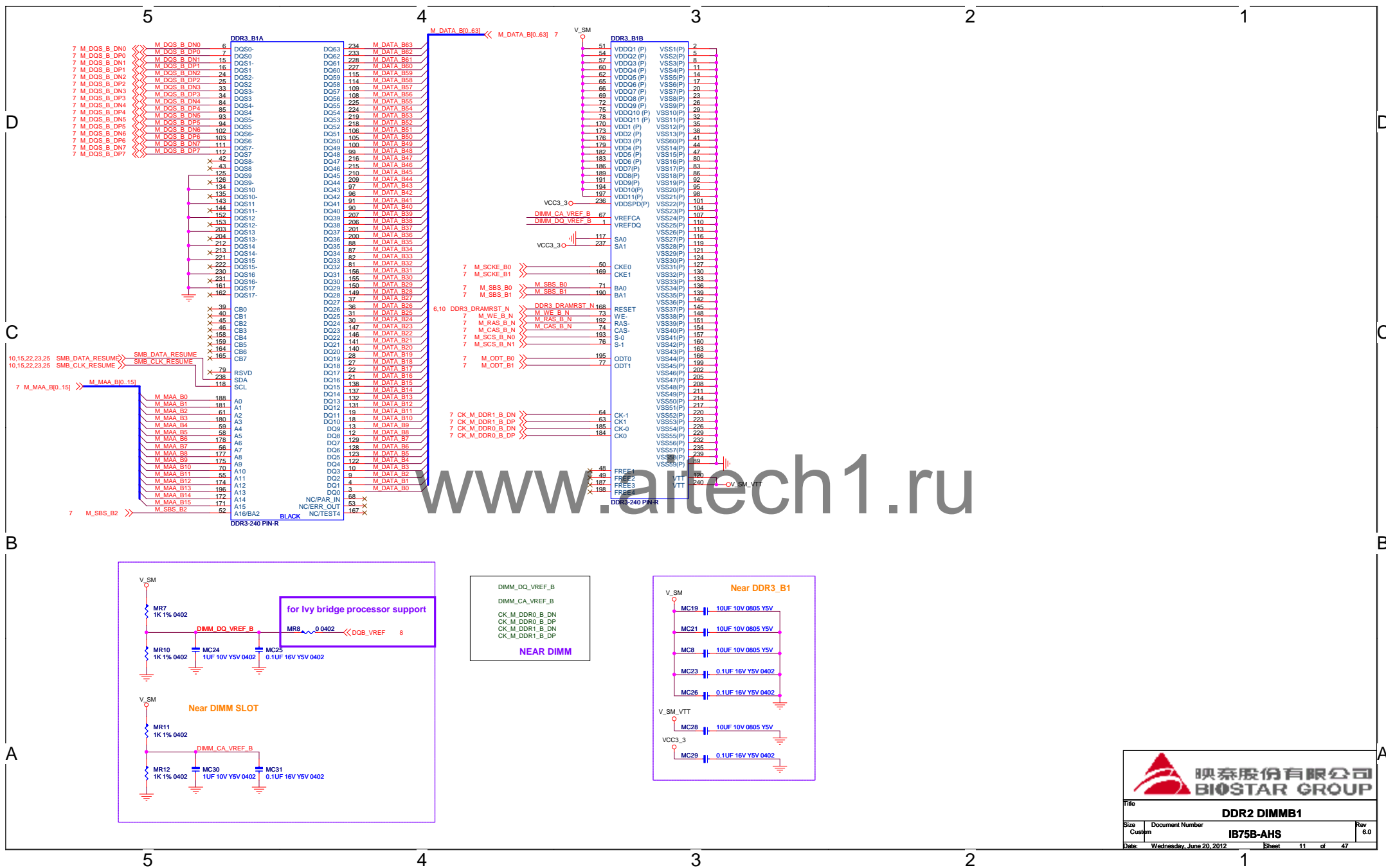
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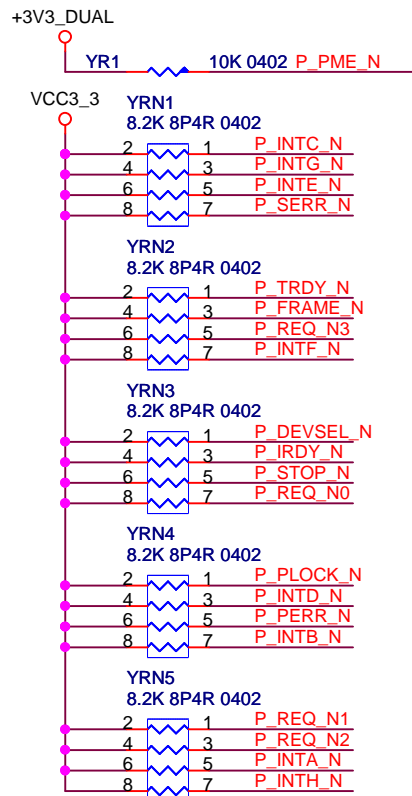
5

4

3

2

1



25 P_PAR

25 P_DEVSEL_N

18 CK_PCH_33M_FB

32 PCH_PCIRST

25 P_IRDY_N

25 P_PME_N

25 P_SERR_N

25 P_STOP_N

25 P_PLOCK_N

25 P_TRDY_N

25 P_PERR_N

25 P_FRAME_N

25 P_GNT_N0

25 P_GNT_N1

25 P_REQ_N0

25 P_REQ_N1

25 P_INTA_N

25 P_INTB_N

25 P_INTC_N

25 P_INTD_N

P_PAR BH8

P_DEVSEL_N BH9

CK_PCH_33M_FB BD15

PCH_PCIRST AV14

P_IRDY_N BF11

P_PME_N AV15

P_SERR_N BR6

P_STOP_N BC12

P_PLOCK_N BA17

P_TRDY_N BC8

P_PERR_N BM3

P_FRAME_N BC11

P_GNT_N0 BA15

P_GNT_N1 AV8

BU12

BE2

P_REQ_N0 BG5

P_REQ_N1 BT5

P_REQ_N2 BK8

P_REQ_N3 AV11

P_INTA_N BK10

P_INTB_N BJ5

P_INTC_N BM15

P_INTD_N BP5

P_INTE_N BN9

P_INTF_N AV9

P_INTG_N BT15

P_INTH_N BR4

PCH1-1

BIOSTAR-D VER:1.2

+Panther Point VER:0.5

PAR

DEVSEL#

CLKIN_PCILOOPBACK

PCIRST#

IRDY#

PME#

SERR#

STOP#

PLOCK#

TRDY#

PERR#

FRAME#

PCI

GNT0#

GNT1#_GPIO51

GNT2#_GPIO53

GNT3#_GPIO55

REQ0#

REQ1#_GPIO50

REQ2#_GPIO52

REQ3#_GPIO54

PIRQA#

PIRQB#

PIRQC#

PIRQD#

PIRQE#_GPIO2

PIRQF#_GPIO3

PIRQG#_GPIO4

PIRQH#_GPIO5

AD0 BF15 P_AD0

AD1 BF17 P_AD1

AD2 BT7 P_AD2

AD3 BT13 P_AD3

AD4 BG12 P_AD4

AD5 BN11 P_AD5

AD6 BJ12 P_AD6

AD7 BU9 P_AD7

AD8 BR12 P_AD8

AD9 BJ3 P_AD9

AD10 BR9 P_AD10

AD11 BJ10 P_AD11

AD12 BM8 P_AD12

AD13 BF3 P_AD13

AD14 BN2 P_AD14

AD15 BE4 P_AD15

AD16 BE6 P_AD16

AD17 BG15 P_AD17

AD18 BC6 P_AD18

AD19 BT11 P_AD19

AD20 BA14 P_AD20

AD21 BL2 P_AD21

AD22 BC4 P_AD22

AD23 BL4 P_AD23

AD24 BC2 P_AD24

AD25 BM13 P_AD25

AD26 BA9 P_AD26

AD27 BF9 P_AD27

AD28 BA8 P_AD28

AD29 BF8 P_AD29

AD30 AV17 P_AD30

AD31 BK12 P_AD31

C_BE0# BN4 P_C/BE_N0

C_BE1# BP7 P_C/BE_N1

C_BE2# BG2 P_C/BE_N2

C_BE3# BP13 P_C/BE_N3

1/10

PANTHERPOINT-B75

P_C/BE_N0 P_C/BE_N0 25

P_C/BE_N1 P_C/BE_N1 25

P_C/BE_N2 P_C/BE_N2 25

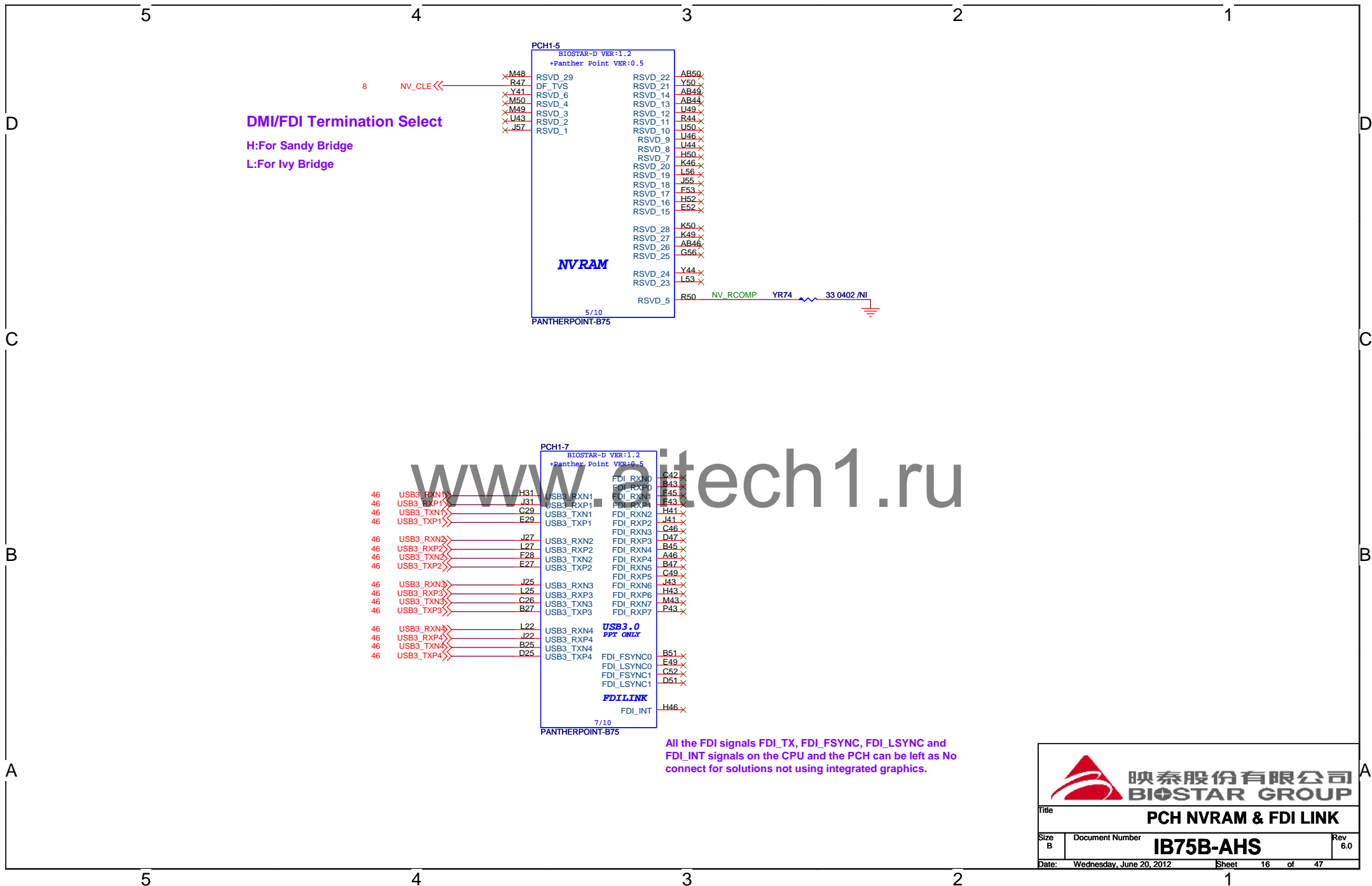
P_C/BE_N3 P_C/BE_N3 25

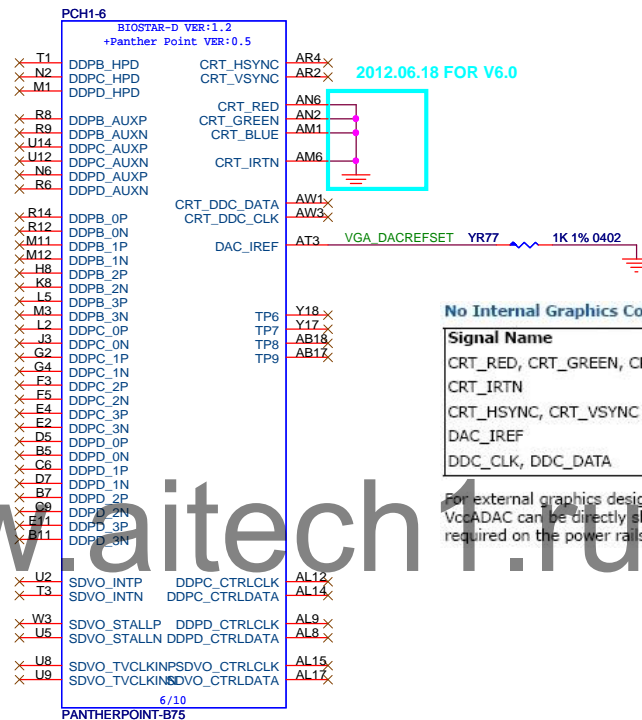
P_AD[31:0] P_AD[31:0] 25

WEAK INTERNAL PULLUPS ON GNT*.DEFAULT SPI BOOT DEVICE

GNT1	GNT0/SATA1GP	BOOT DEVICE
0	0	LPC
0	1	NANO
1	0	PCI
1	1	SPI

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Title PCH PCI		
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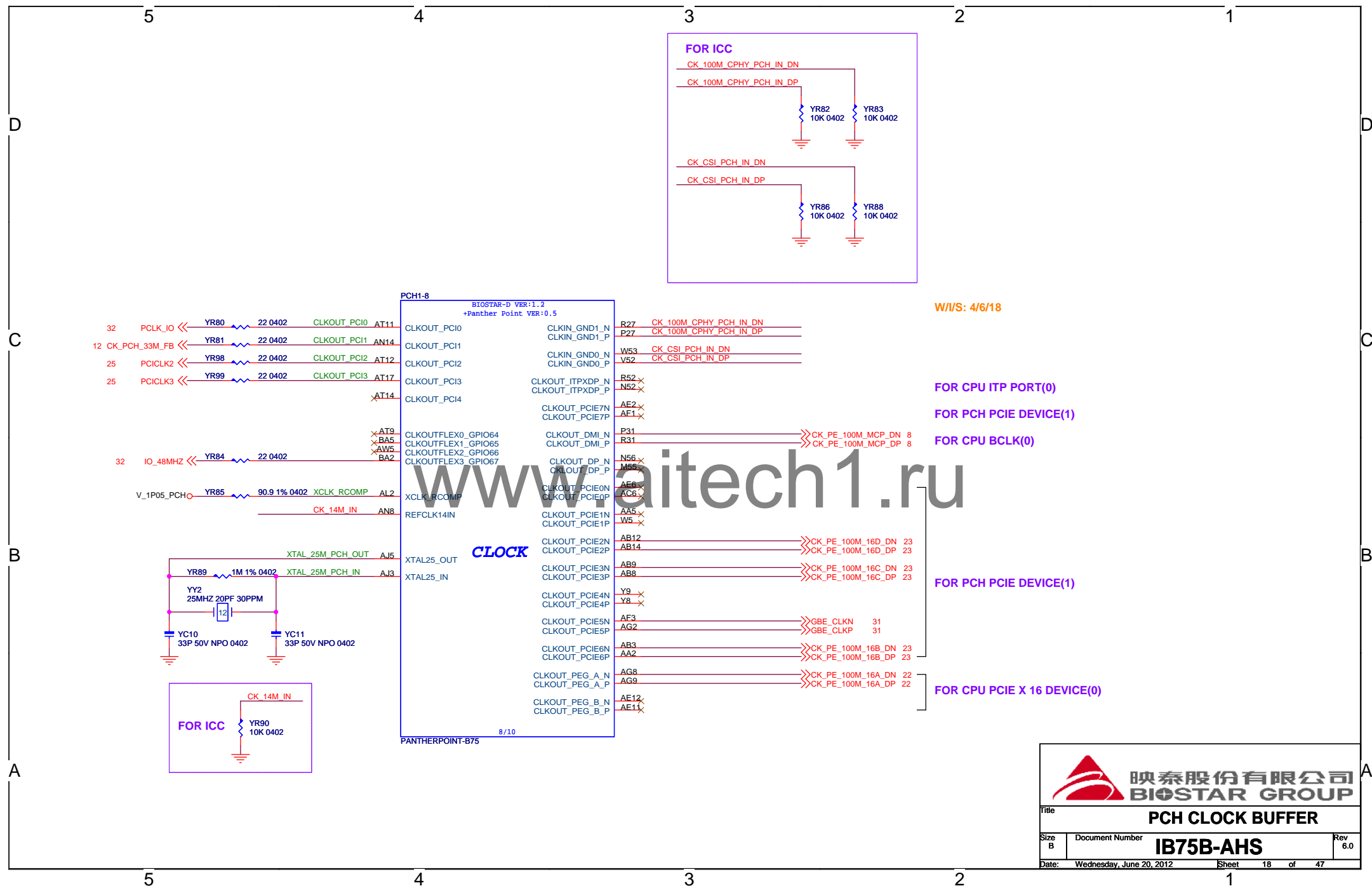
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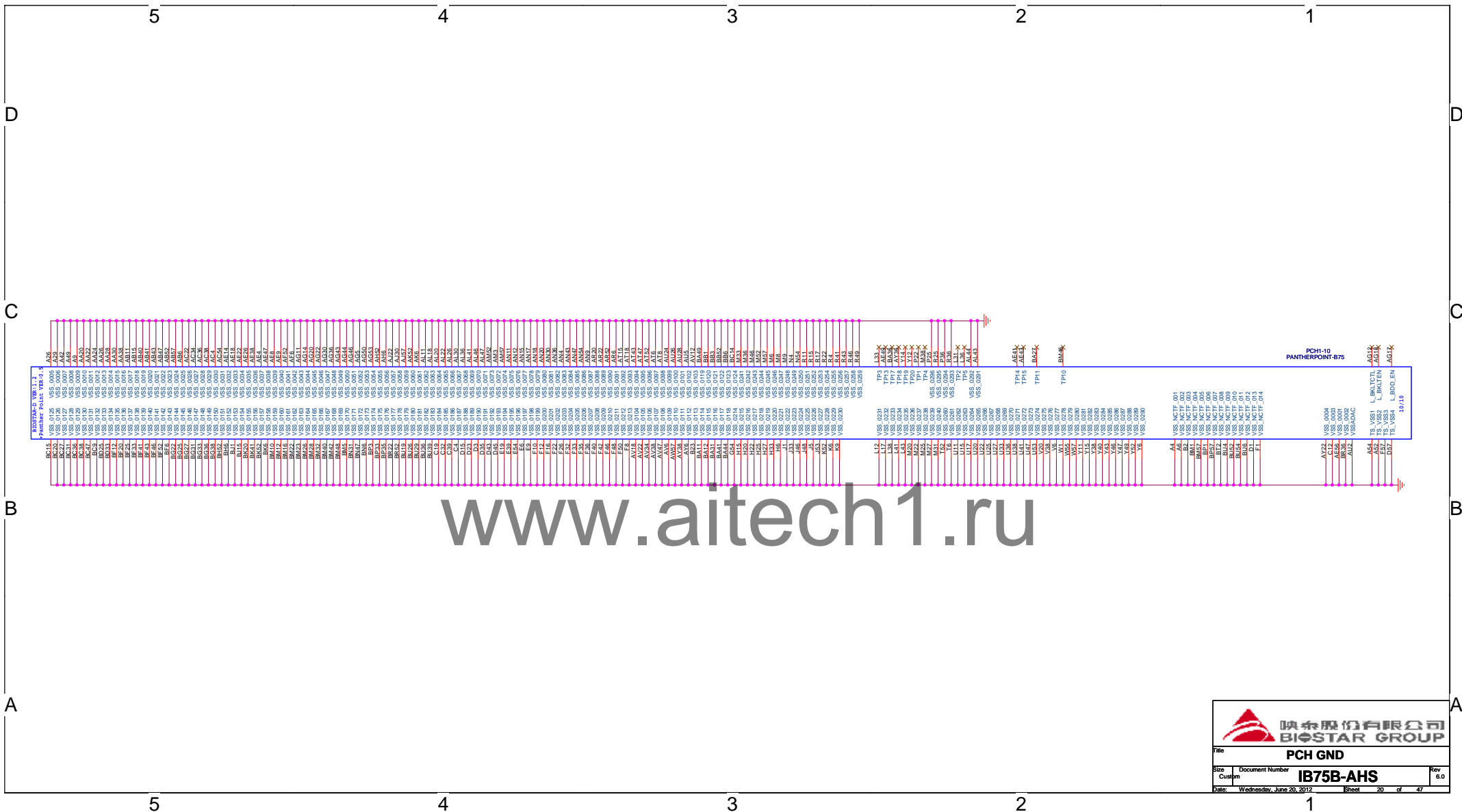
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Title: PCH VGA/DISPLAY PORT

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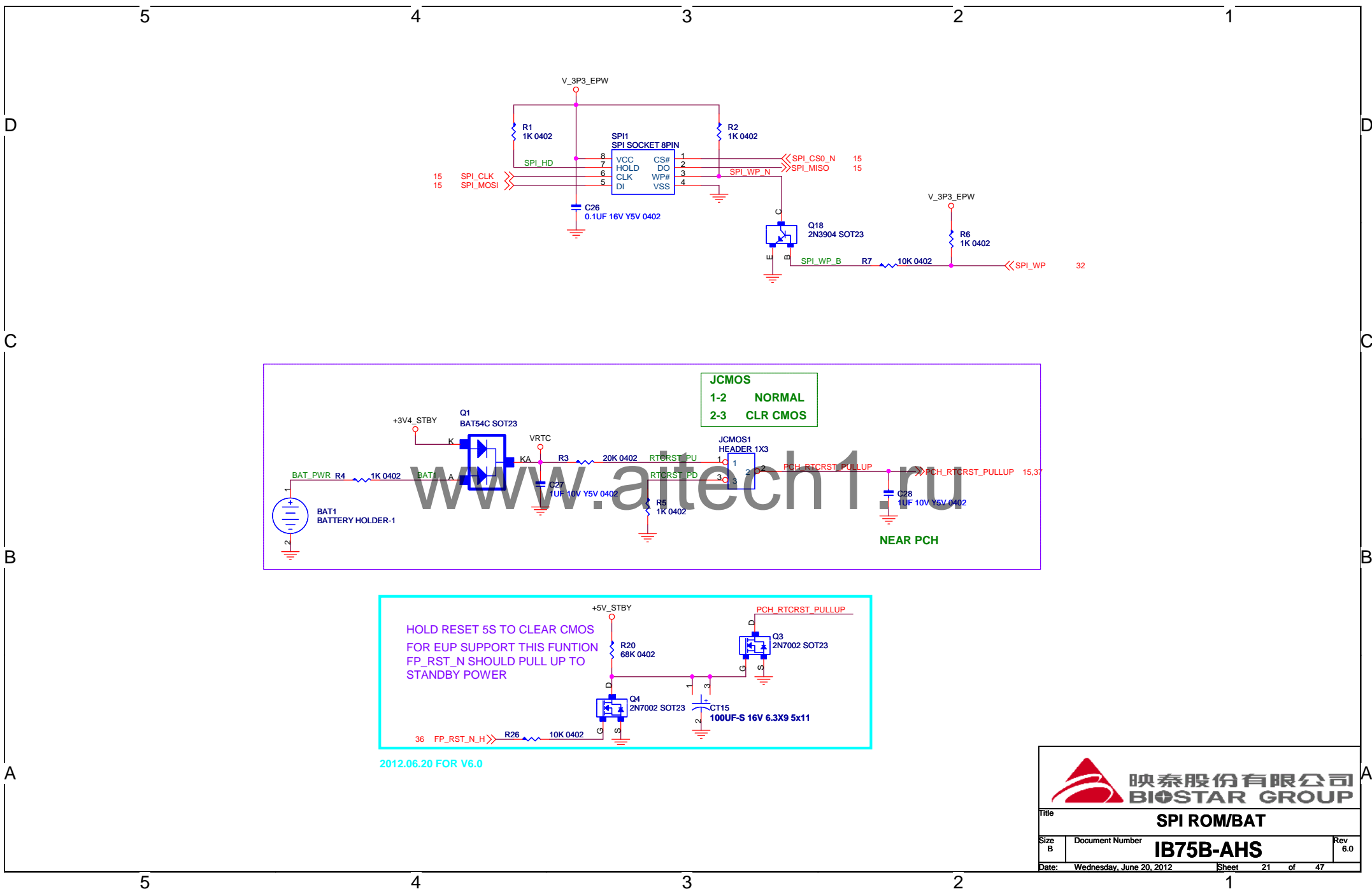
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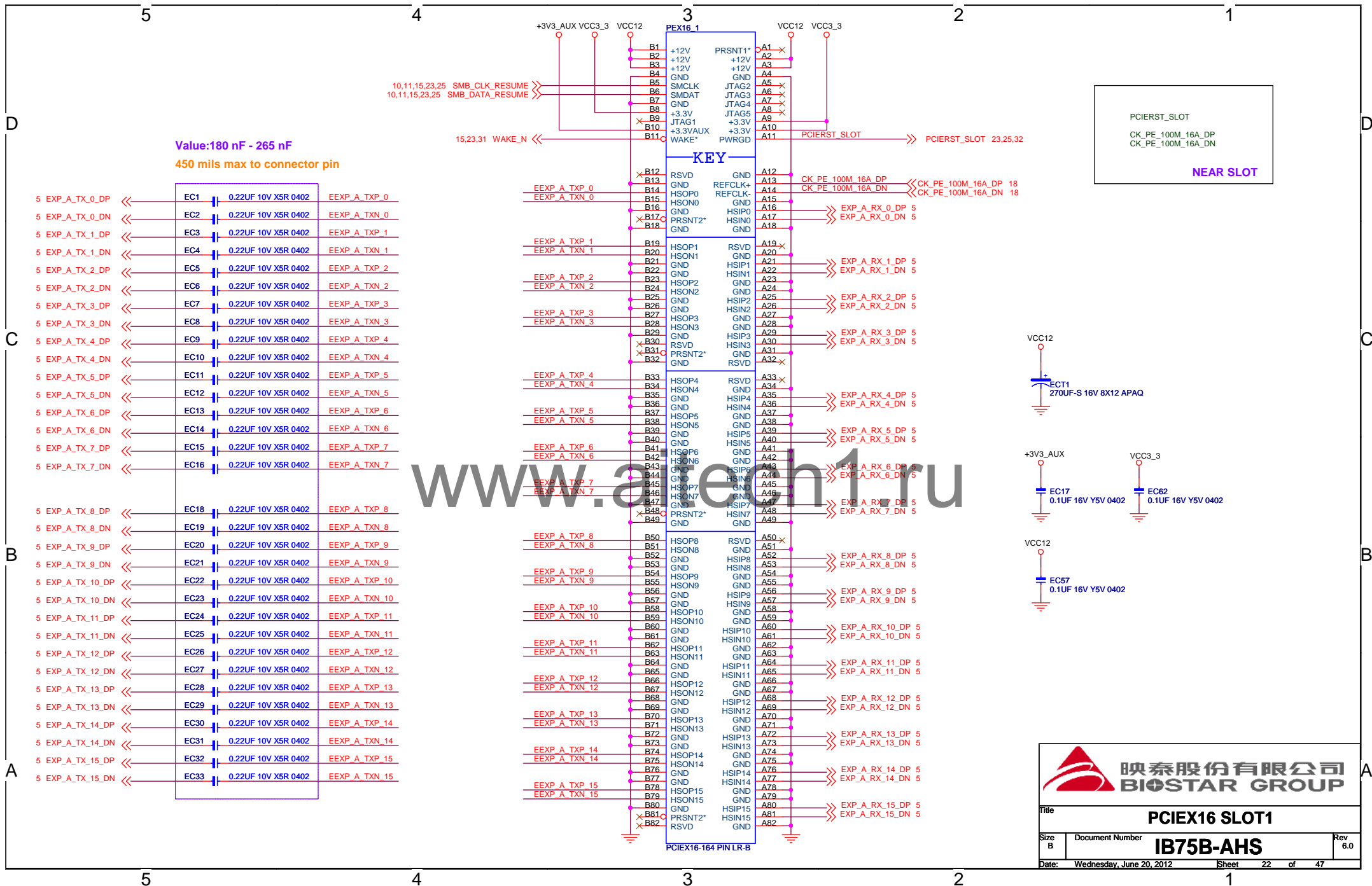


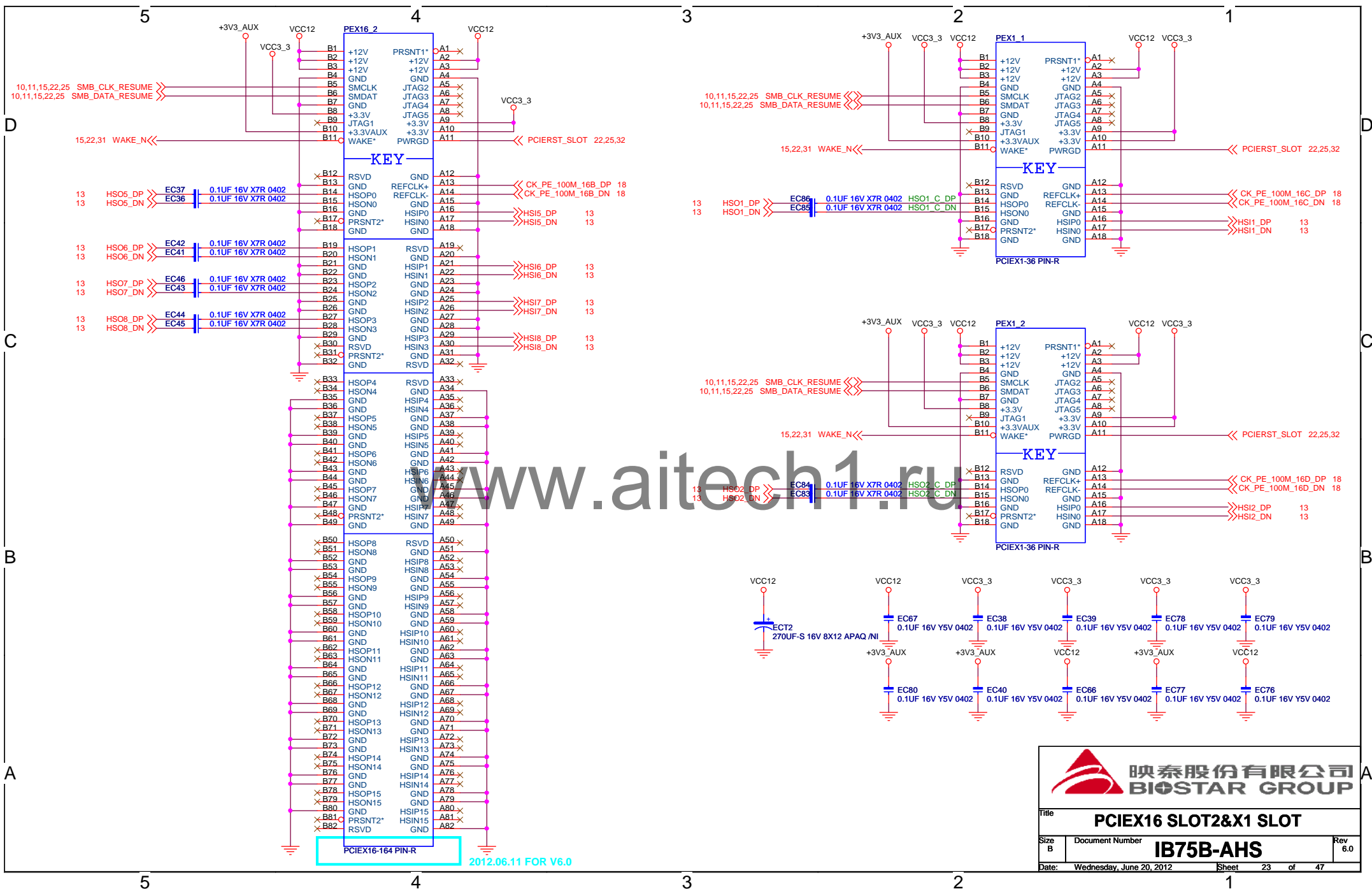



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Title: PCH GND			
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Title: **PCIEX16 SLOT2&X1 SLOT**

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Title		VGA	
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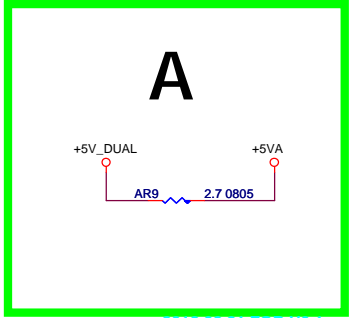
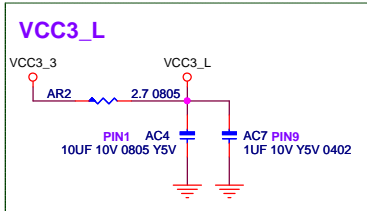
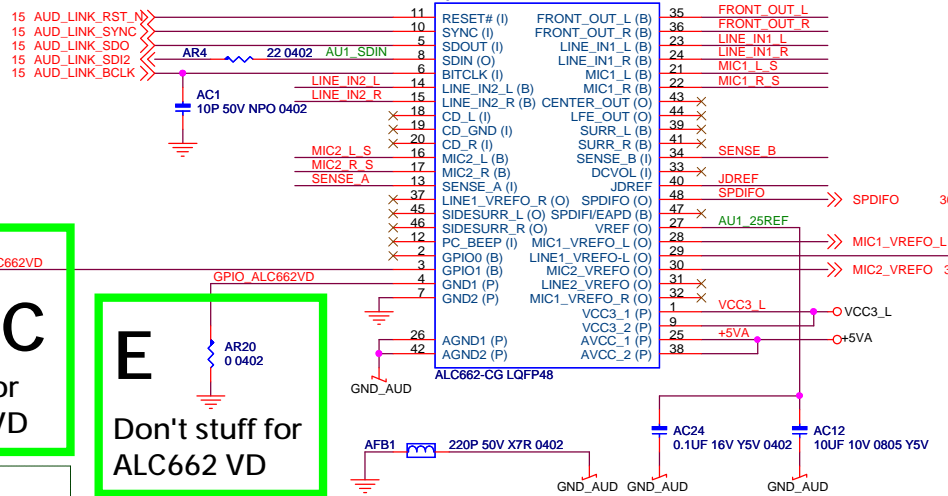
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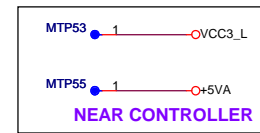
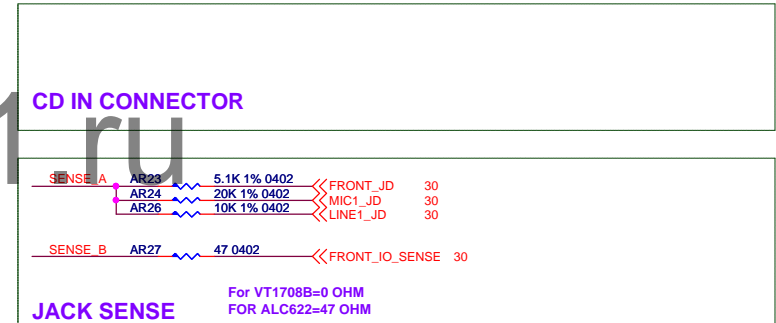
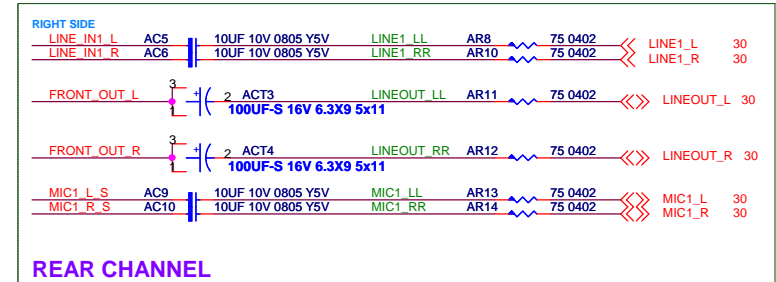
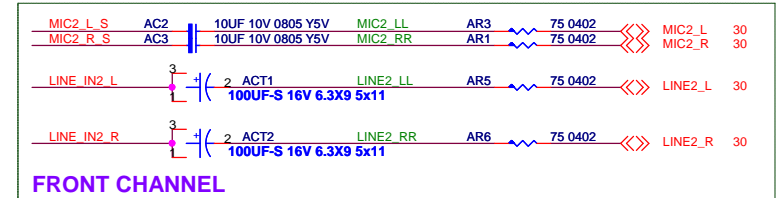
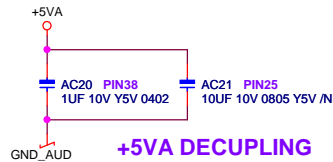
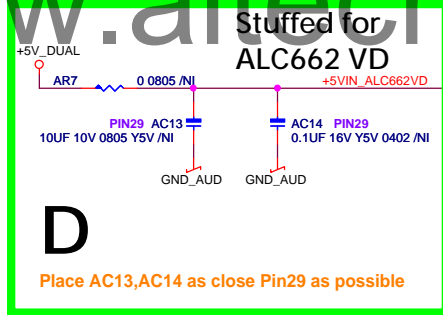
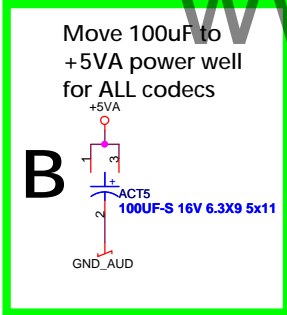
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AUDIO PART: A+Reference

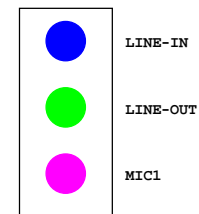
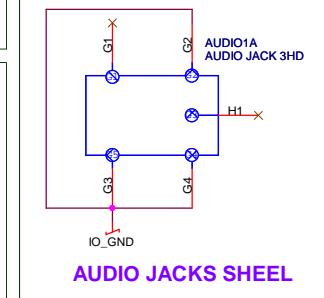
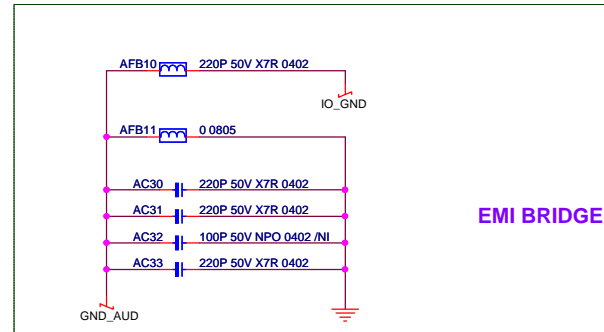
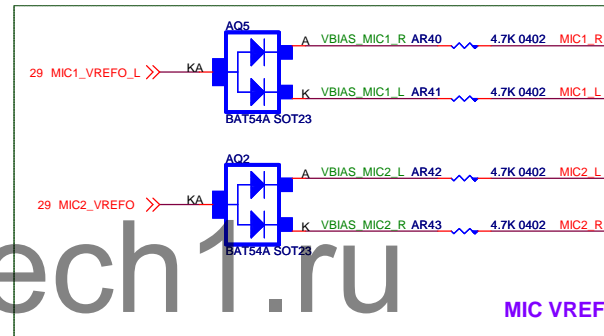
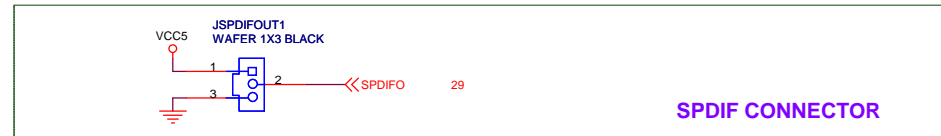
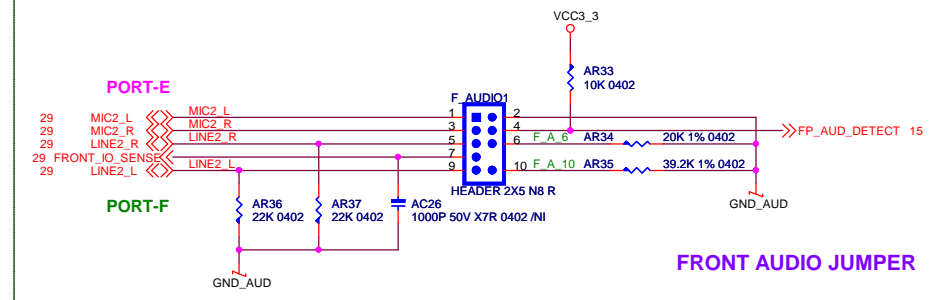
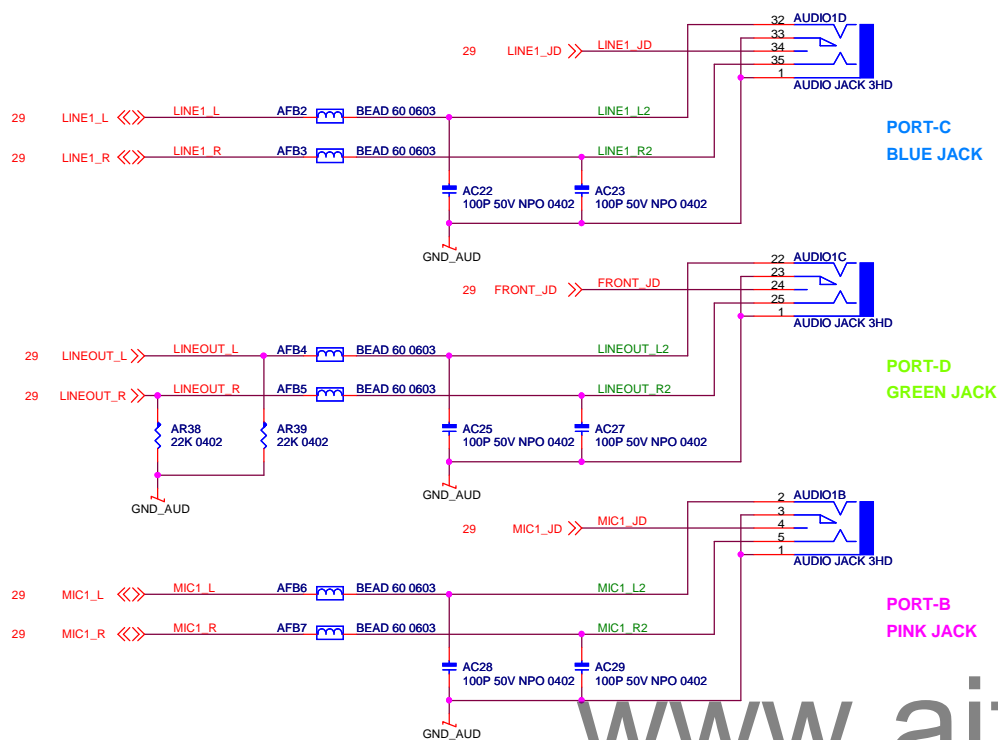


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Title CODEC ALC662		
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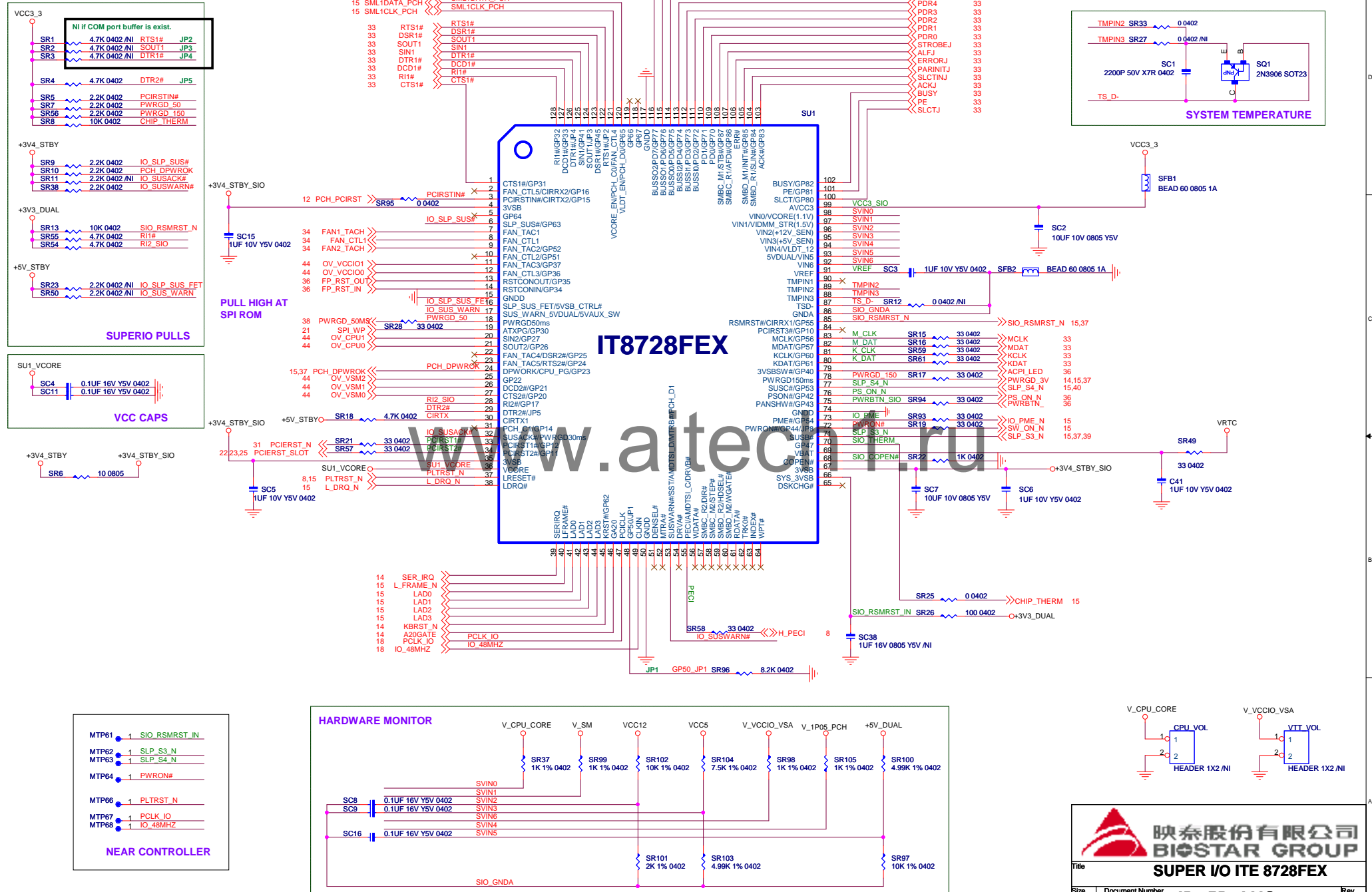
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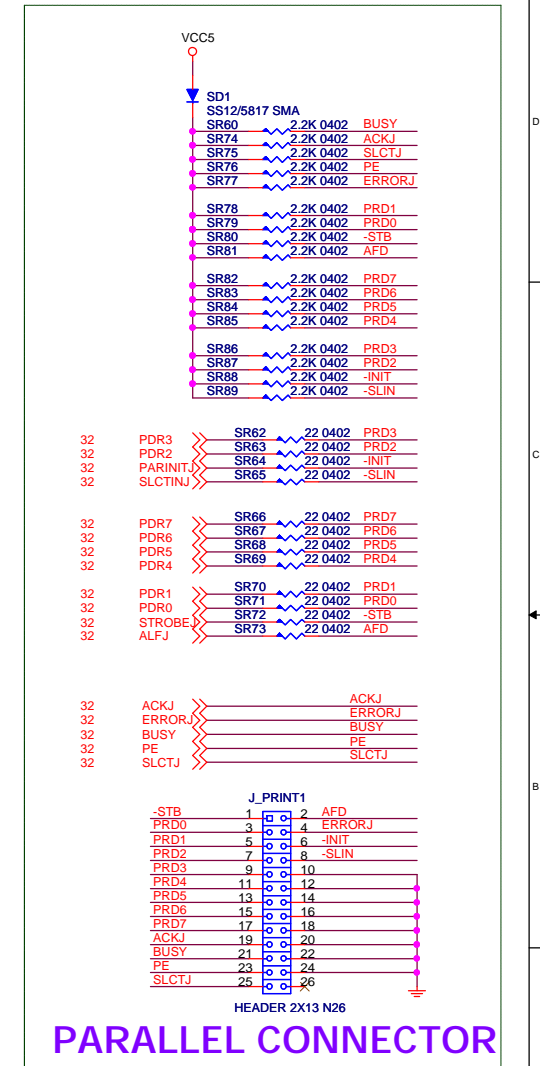
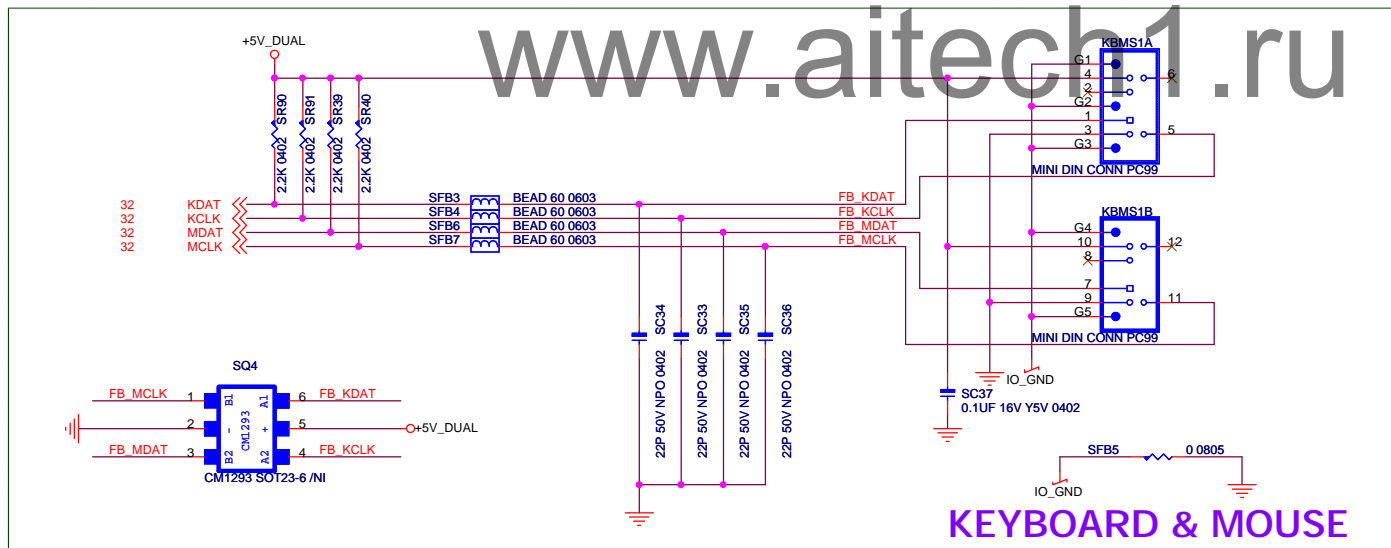
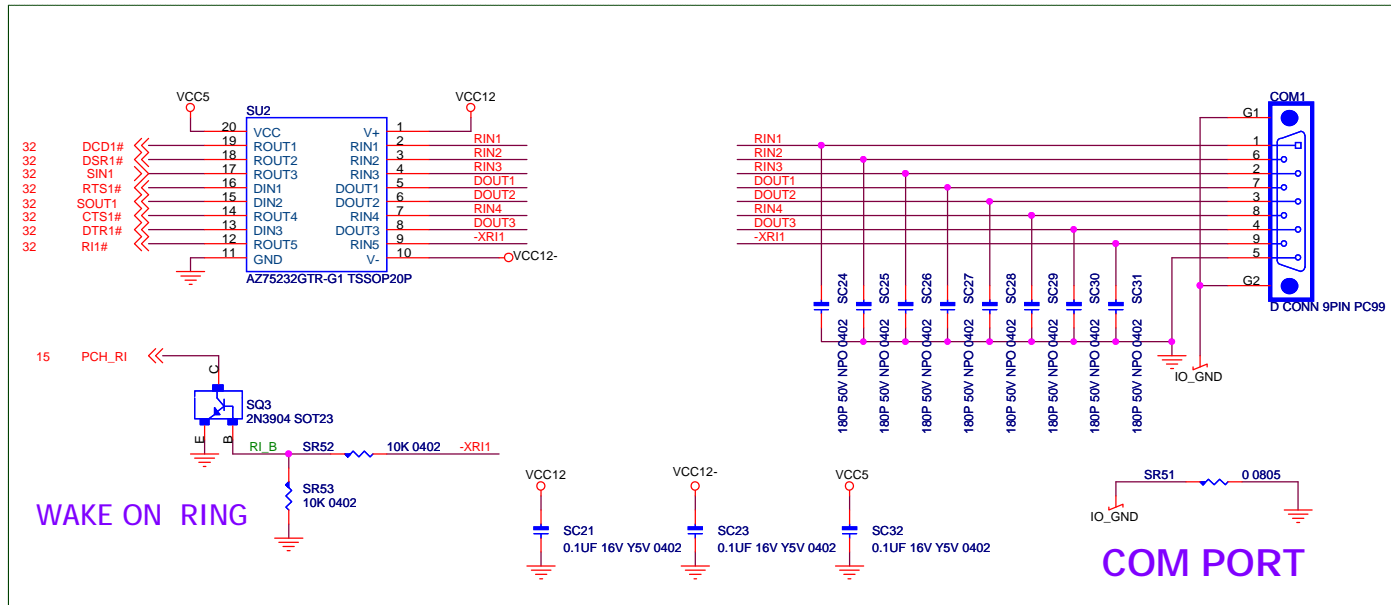
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SUPERIO PART: S+Reference





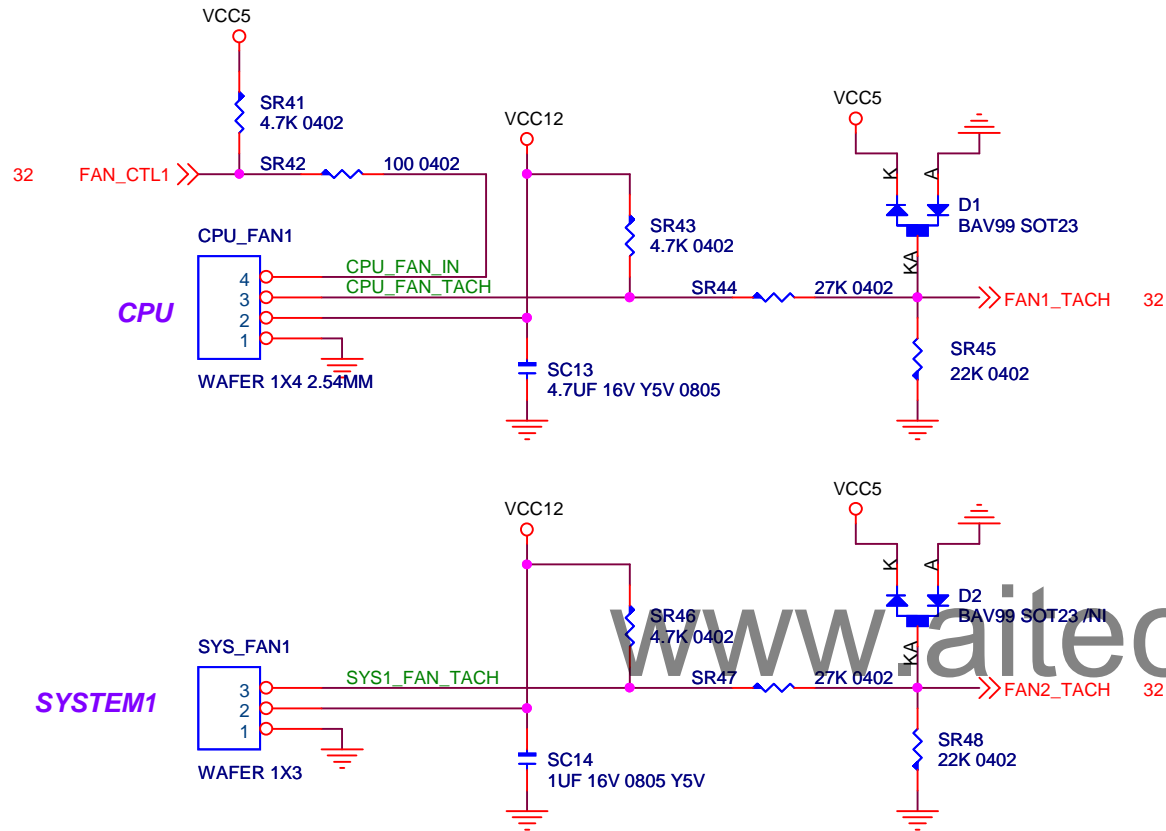
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Title: **COM/PRINTER/PS2 CONN**

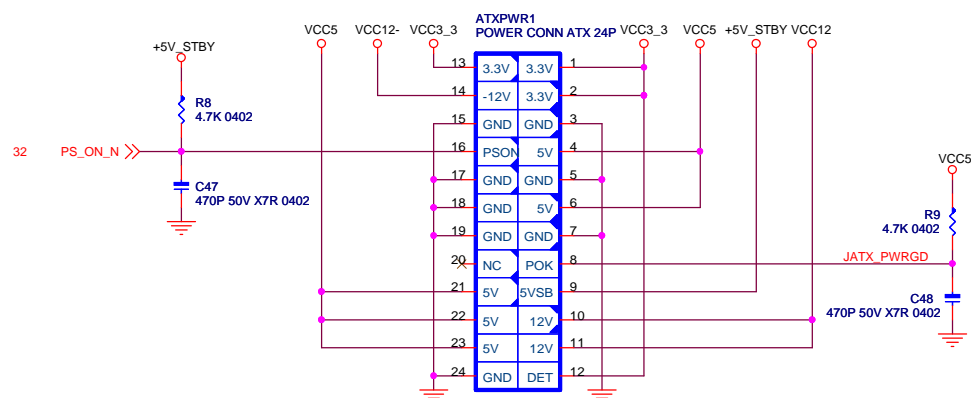
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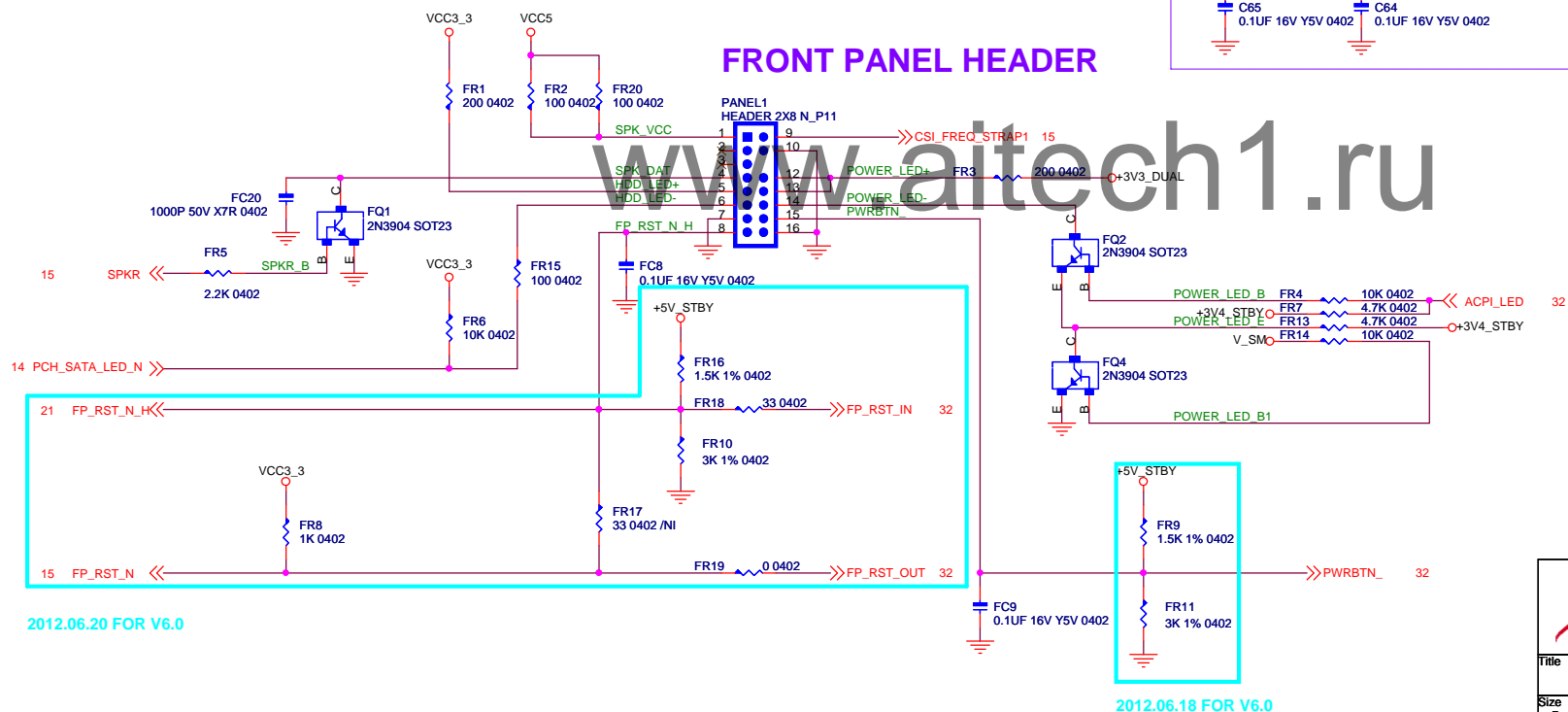
CPU FAN/SYSTEM FAN1



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JATXPWR

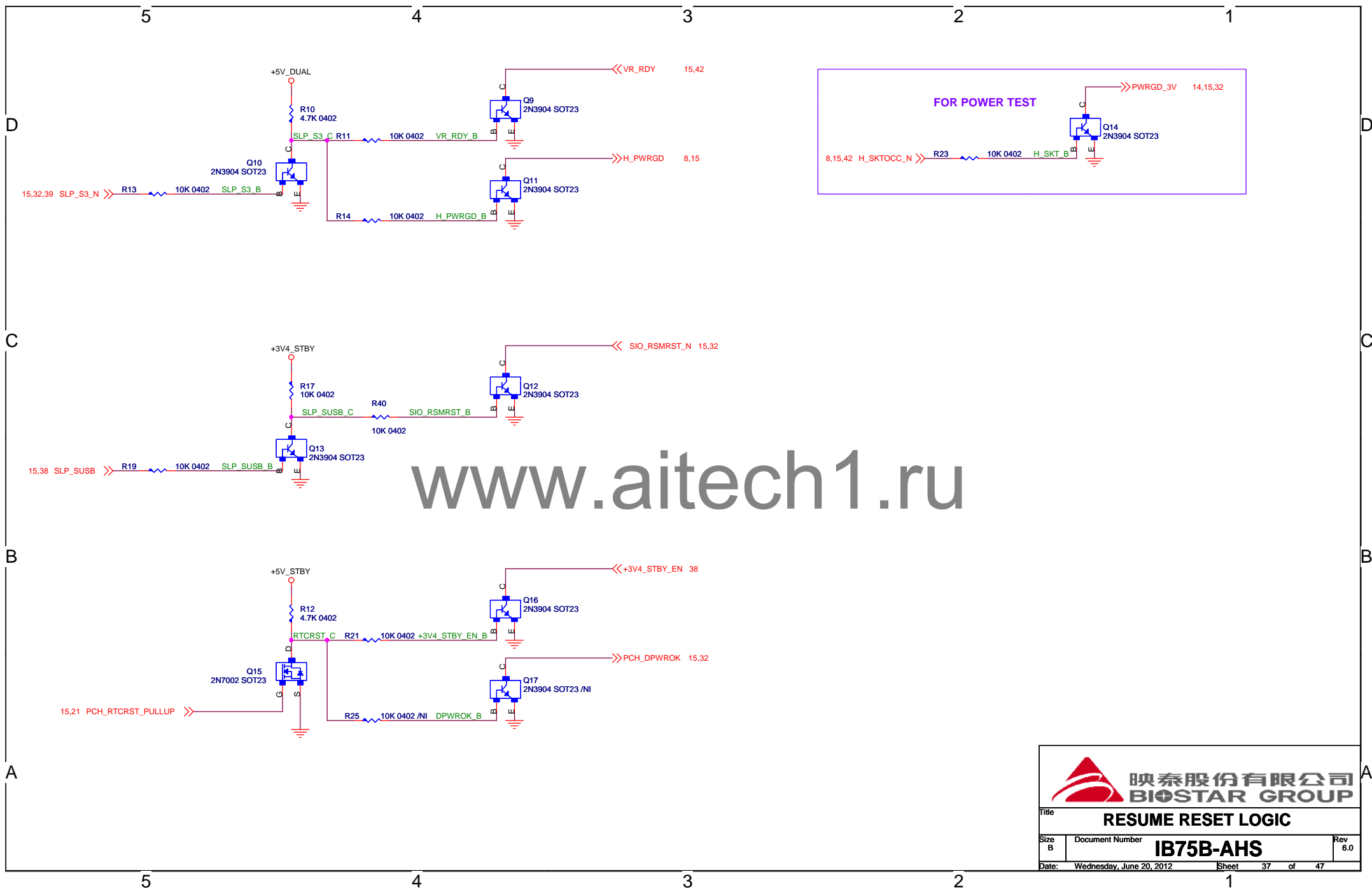
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2012.06.20 FOR V6.0

2012.06.18 FOR V6.0

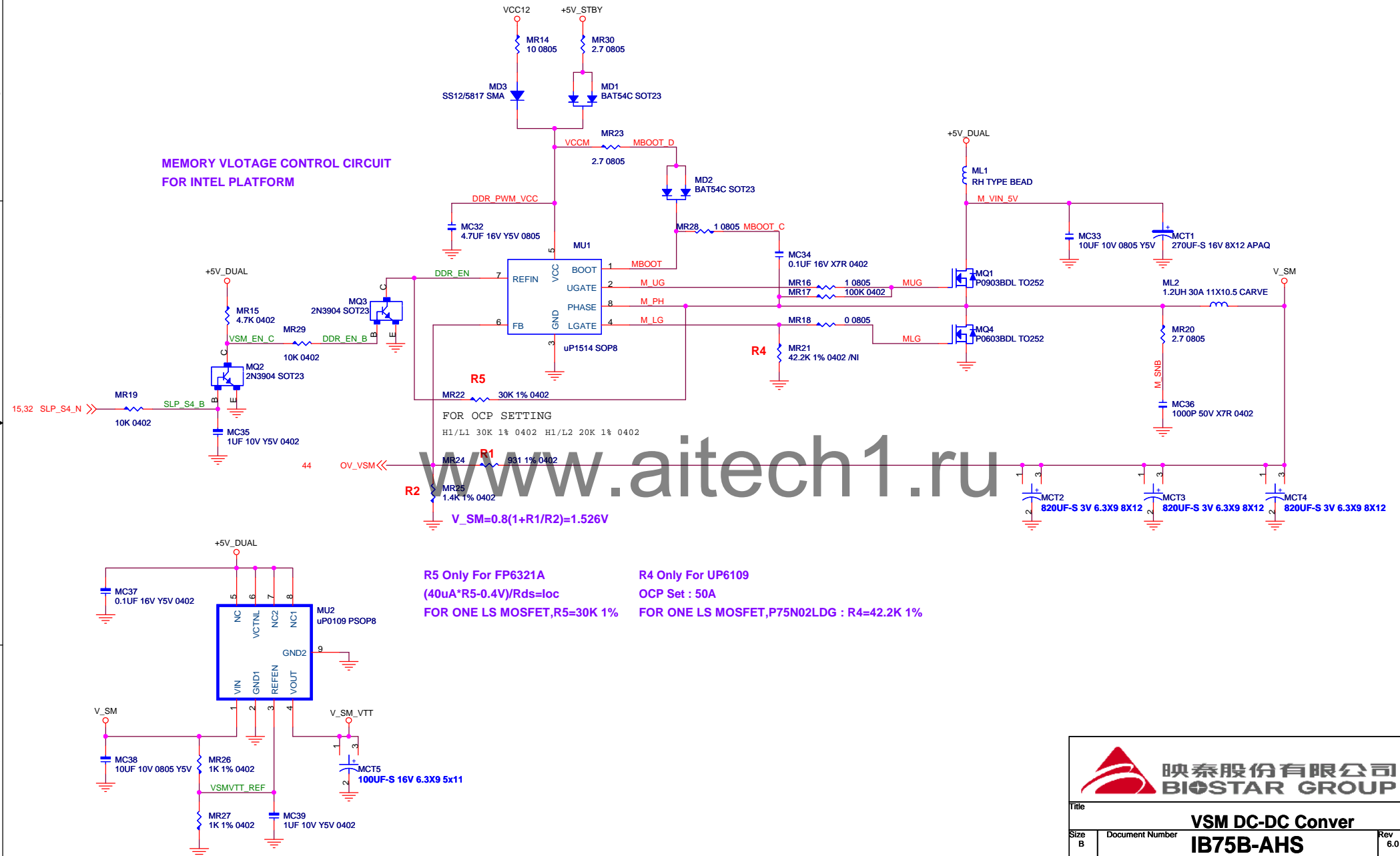




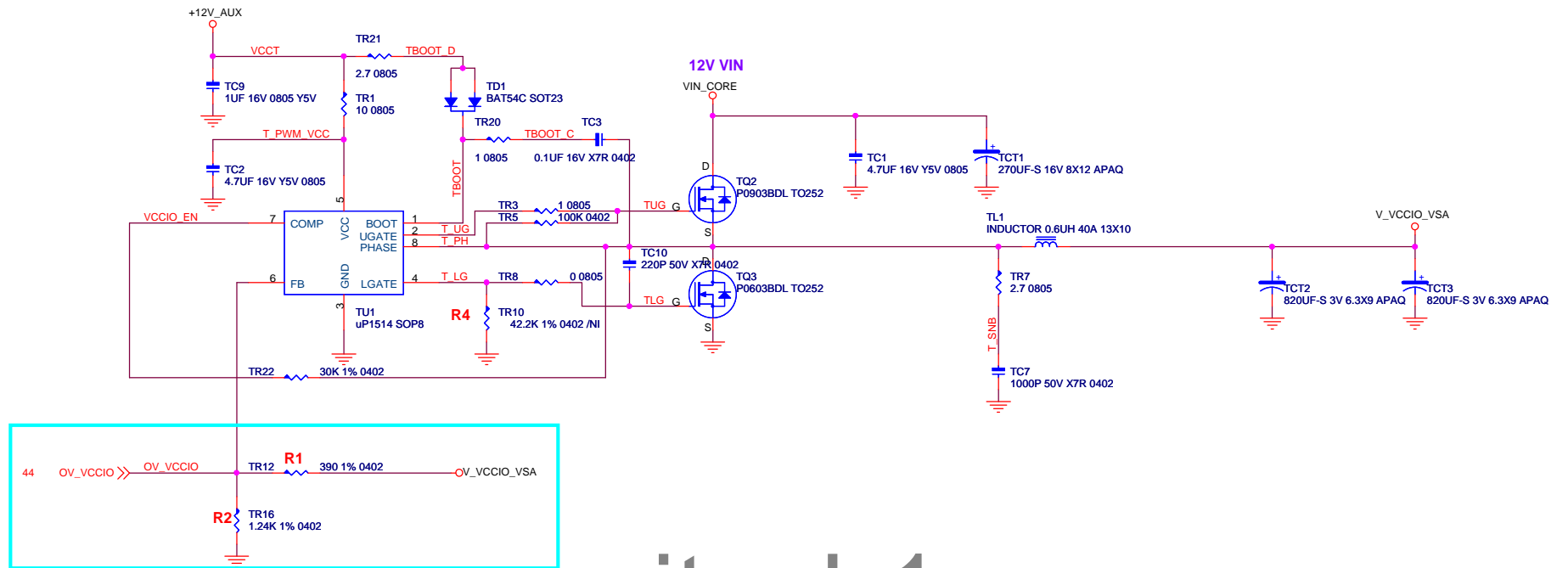
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Title RESUME RESET LOGIC			
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MEMORY VOLTAGE CONTROL CIRCUIT FOR INTEL PLATFORM

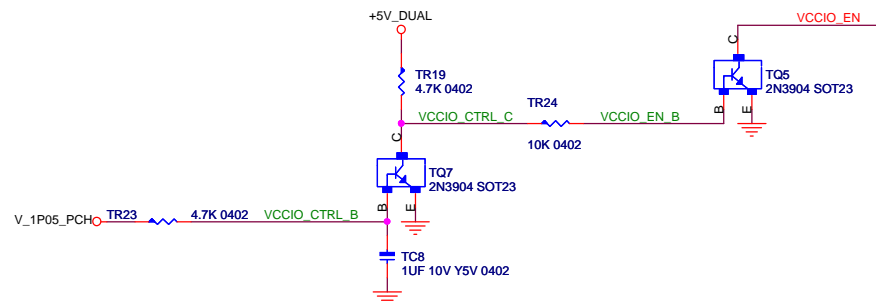



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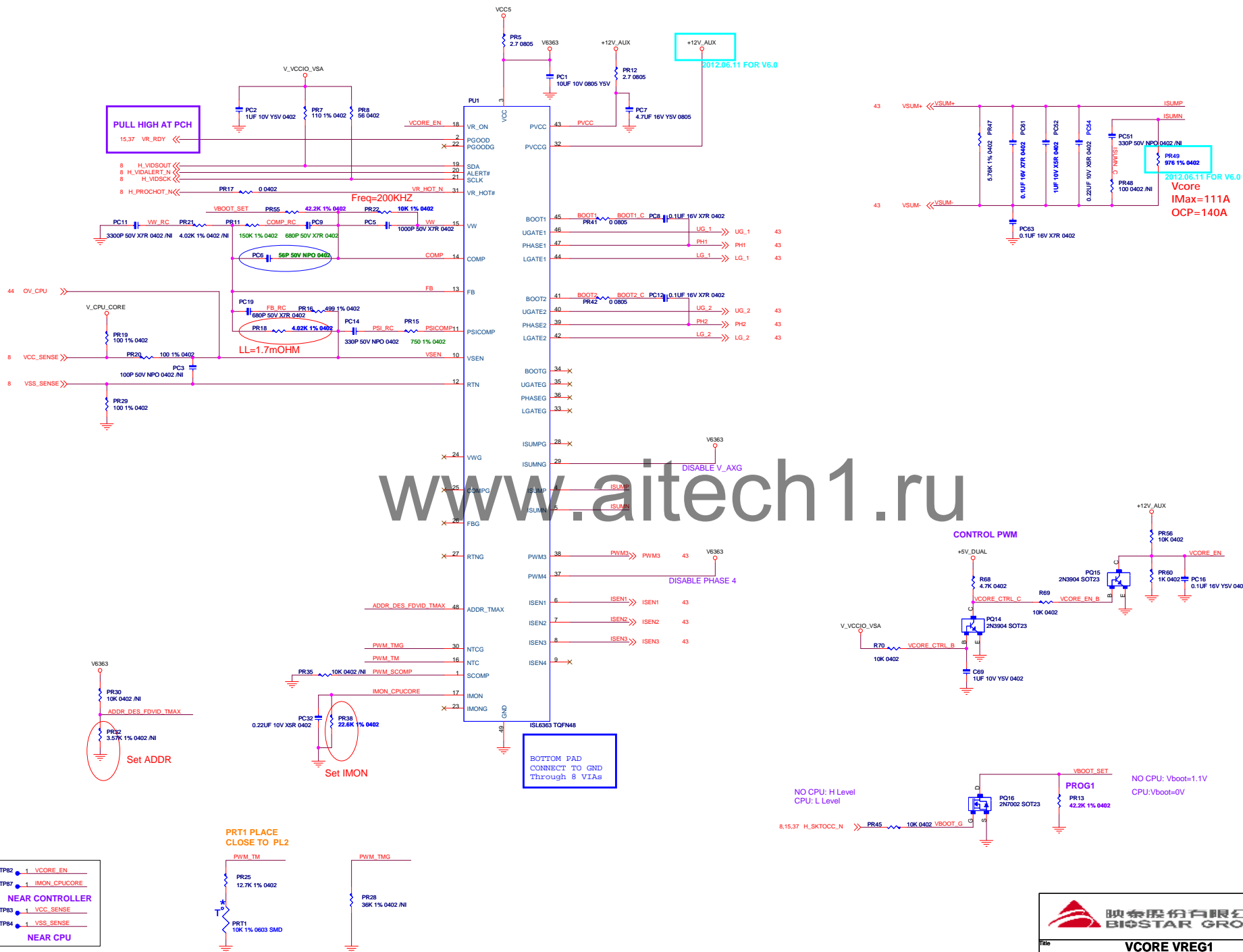


2012.06.11 FOR V6.0

$V_{out} = 0.8V \times (1 + R1/R2) = 1V$
 R4 Only For UP6109
 OCP Set : 50A
 FOR TWO LS MOSFET,P0903BDG : R4=26.1K 1%

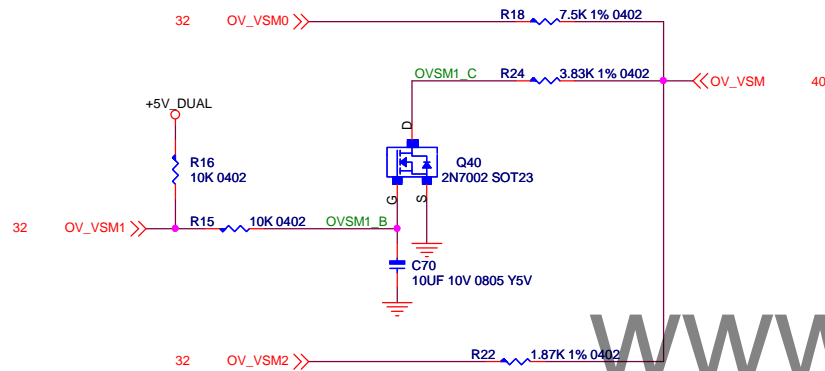


			
Title			
VTT DC-DC Conver			
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V_CPU_VCCIO	OV_VCCIO0	OV_VCCIO1
1.05V(DEFAULT)	1	1
1.15V	0	1
1.25V	1	0
1.35V	0	0



V_SM	OV_VSM0	OV_VSM1	OV_VSM2
1.3V(1.332)	1	0	1
1.4V(1.431)	0	0	1
1.5V(DEFAULT)(1.526)	1	1	1
1.6V(1.625)	0	1	1
1.7V(1.730)	1	0	0
1.8V(1.829)	0	0	0
1.9V(1.924)	1	1	0

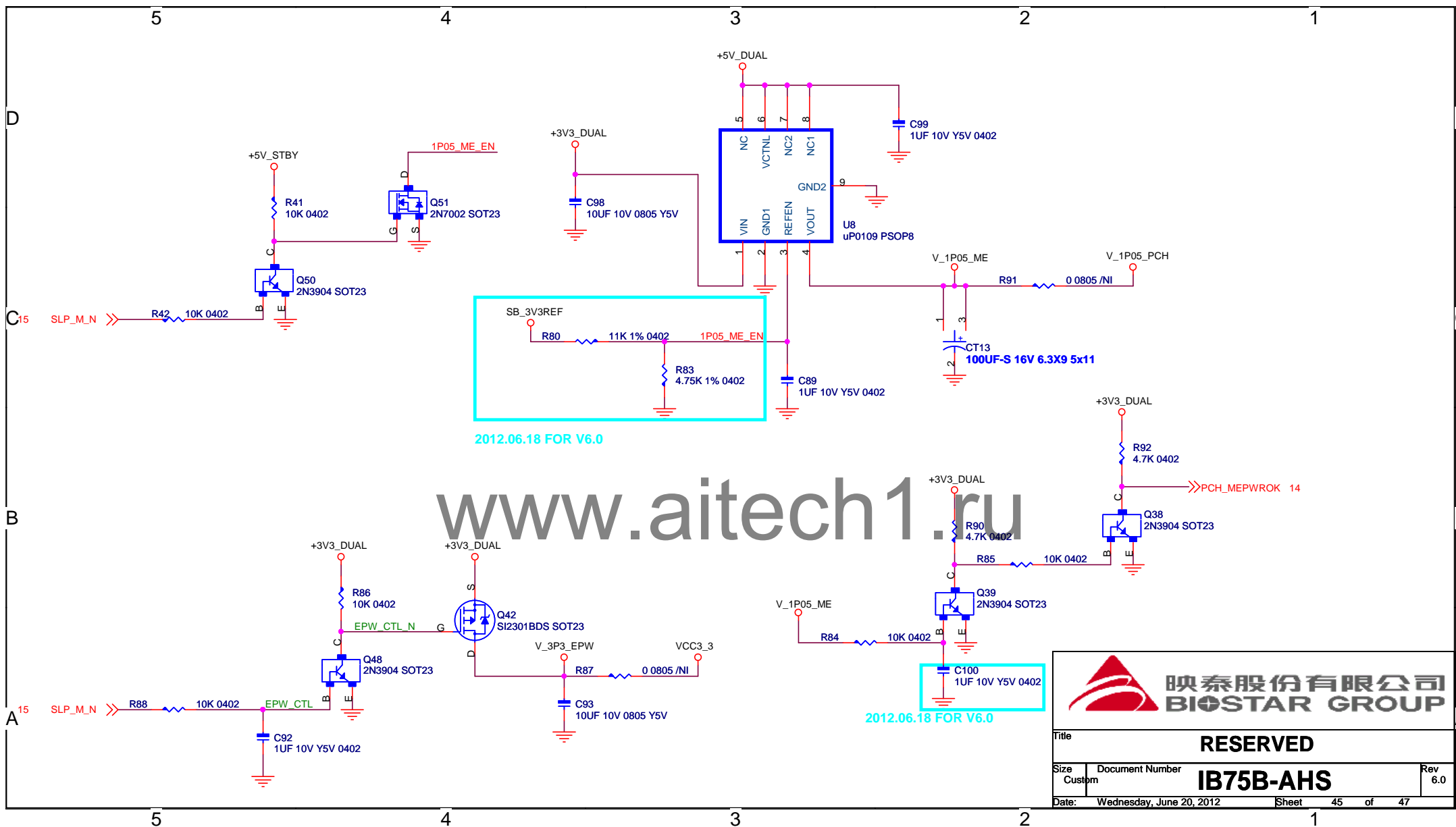


V_CPU_CORE	OV_CPU0	OV_CPU1
DEFAULT	1	1
+5%	0	1
+10%	1	0
+15%	0	0



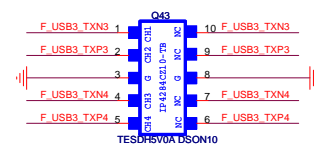
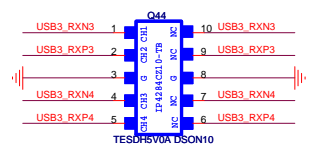
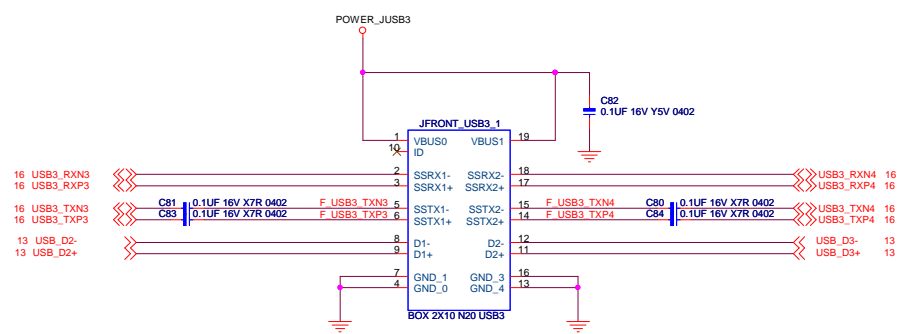
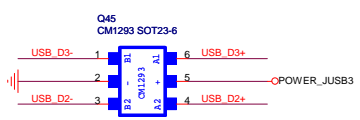
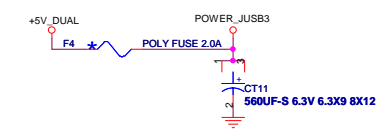
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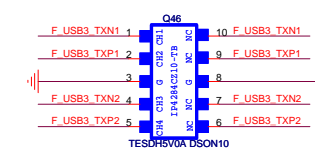
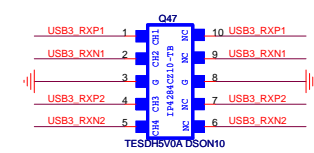
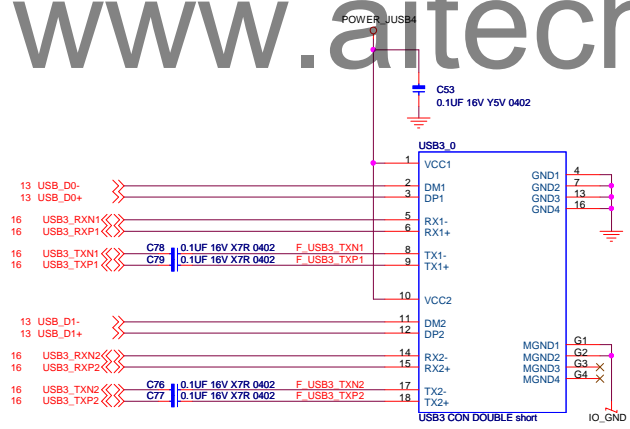
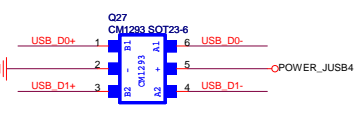
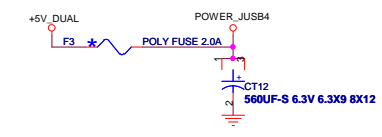


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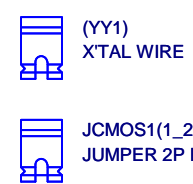
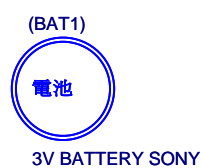
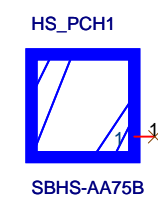
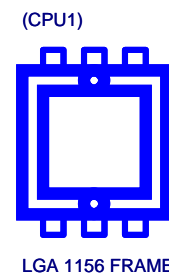
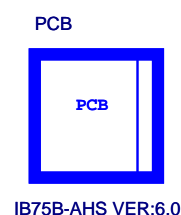
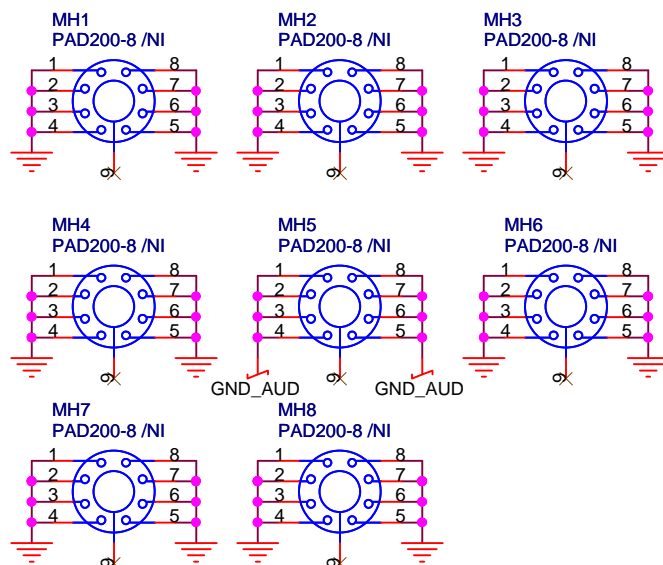


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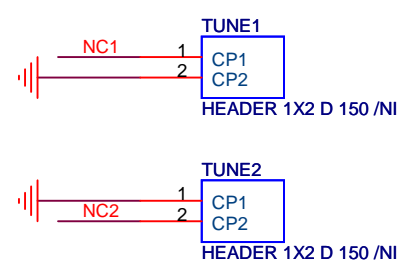
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